Editors' Notes

GROUND, REGULATORS, AND GAMES

The difficulty of maintaining true ground has been discussed in these pages numerous times, usually in terms of ac and dc behavior. However, circuits such as buck- and boost regulators that rapidly and repeatedly switch large amounts of current, can cause large *transient* ground errors. The origin of this "ground-bounce" phenomenon is explained in easy-to-understand terms, leading logically to a sensible PC-card design approach that minimizes the transients—starting on Page 3.

A *low-dropout regulator* (LDO) is a handy way to immunize a circuit against the battery discharge curve when the upstream voltage becomes so low that the output voltage of a conventional regulator would begin to drop. Some of the fine points of LDO design are discussed in the article starting on Page 8.

NEW FELLOWS NAMED

Dr. Colin Lyden and Dr. Zoran Zvonar have been elevated to the distinguished position of ADI Fellow during our 2007 General Technical Conference, which attracted approximately 1,900 engineers from the company's design sites worldwide.

The Fellows honor is bestowed on a select group of engineers who have contributed significantly to ADI's business and demonstrated important qualities, such as innovation, leadership, entrepreneurial ability, and consulting skills. In addition, an ADI Fellow must be a company ambassador, bridging across organizations and demonstrating an unparalleled ability to teach and mentor others within the company. With the latest inductions in this, the program's 27th year, Analog Devices has a total of 33 Fellows within our community of 3,500 engineers worldwide.

"Engineering excellence and innovation continue to set ADI apart," said Sam Fuller, vice president of Research and Development. "We are fortunate that exceptional engineers like Colin and Zoran, who are recognized both inside and outside the company for their expertise, have chosen to make their careers at Analog Devices. Their work has challenged the conventional wisdom within the company, extended our ambitions for new-product performance, and served as an inspiration for the next generation of engineers to sustain ADI's record of innovation."

Colin Lyden received his Ph.D. in 1984 from University College, Cork, Ireland. He joined ADI in 1999 as an engineering director with leadership responsibility for the Limerick CAD group and the Cork Design Centre. His creative ideas and work, blurring the traditional distinctions between sigma-delta, successive-approximation, and pipelined converter architectures, have resulted in performance improvements in a range of ADI products, including the AD7982 and the AD7767 successive-approximation analog-to-digital converters.

Colin, who holds 15 U.S. patents, was the lead architect for a new CT medical-imaging analog front end that achieved breakthroughs in both cost and performance—and has been designed into next-generation high-slice CT machines.

Zoran Zvonar, having earned his Ph.D. at Boston's Northeastern University in 1993, joined ADI in 1994 as one of the company's first system engineers to specialize in communications algorithms. An expert in wireless system design for varied communications applications, Zoran has extensively published in leading technical journals. He also serves as an editor for the *IEEE Communications Magazine* and is co-author of several books focusing on GSM and third-generation wireless communications systems.

Zoran developed and validated a breakthrough system approach for wireless handsets that resulted in two patents and enabled *direct conversion*—the process of converting analog RF signals directly to digital baseband data—to be applied successfully to the GSM wireless communications standard. He was a member of the core technology design team for ADI's SoftFone® and Othello® wireless product families.

Dan Sheingold [dan.sheingold@analog.com]

GPS NAVIGATION

In November, I purchased an inexpensive aftermarket GPS navigation system for my car. The system can be helpful, even in well-known locations, where it alerts me to upcoming turns, can plot a scenic route on one of the parkways, and occasionally teaches me a new shortcut. It's also entertaining on long road trips, where it continually counts down the remaining miles and minutes, its highly visible progress display making it seem that the destination is closer than it actually is. Its main purpose, of course, is plotting a course to an unfamiliar location. The combination of audio and visual clues makes finding addresses easy, and the routing options provide a simple way to choose the shortest route—or the quickest route—to avoid toll roads or local roads, and to navigate around a detour.

The hidden beauty, however, is using the extensive collection of points-of-interest to show what's available in an unknown area. Recently, a friend from Connecticut met me in Charlestown, Rhode Island, a town that is roughly halfway between our houses. Neither of us was familiar with the area. Upon arrival, we found that the restaurant that we had chosen for lunch was closed. No worries—the GPS showed us several other local restaurants, as well as the town beach, two National Wildlife Refuges, and a seventeenth-century gristmill. It helped us to enjoy a day trip in a beautiful, if unfamiliar town.

I have three complaints about this low-end GPS, however. The first, and most serious, is that the touch screen is becoming less responsive as the summer temperatures in New England continue to rise. A few minutes in front of the air-conditioning outlet usually cures the problem, but I'm a fan of sunshine and open roofs. Too bad the manufacturer didn't use an ADI capacitance-to-digital converter, which includes on-chip calibration logic to compensate for changes in temperature and humidity.

The second problem is that the GPS loses its signal when I travel through Boston's Big Dig tunnels, making it unable to maintain its bearings or to provide instructions for lane splits and exits. Too bad it doesn't include an ADI accelerometer, whose inertial navigation capabilities could provide positional information during these temporary signal losses.

The third minor irritation is that the aftermarket GPS has no connection to the car stereo, and thus cannot mute the music when it needs to provide spoken directions. Fortunately, my system gives several warnings before each turn, allowing me to turn the radio down when necessary.

Readers: What are the best features of your GPS, or your pet peeves with your systems? Designers: What should we be looking for in next-generation systems? Your comments are welcome.

Scott Wayne [scott.wayne@analog.com]

Analog Dialogue

www.analog.com/analogdialogue **dialogue.editor@analog.com**

Analog Dialogue is the free technical magazine of Analog Devices, Inc., published continuously for 41 years—starting in 1967. It discusses products, applications, technology, and techniques for analog, digital, and mixed-signal processing. It is currently published in two editions—*online*, monthly at the above URL, and quarterly *in print*, as periodic retrospective collections of articles that have appeared online. In addition to technical articles, the online edition has timely announcements, linking to data sheets of newly released and pre-release products, and "Potpourri"—a universe of links to important and rapidly proliferating sources of relevant information and activity on the Analog Devices website and elsewhere. The *Analog Dialogue* site is, in effect, a "high-pass-filtered" point of entry to the **www.analog.com** site—the virtual world of *Analog Devices*. For history buffs, the *Analog Dialogue* archives include all regular editions, starting with Volume 1, Number 1 (1967), plus three special anniversary issues.

If you wish to subscribe to the print edition, please go to **www.analog.com/analogdialogue** and click on **<subscribe>**. Your comments are always welcome; please send messages to **dialogue.editor@analog.com** or to these individuals: *Dan Sheingold*, Editor **[dan.sheingold@analog.com]** or *Scott Wayne*, Managing Editor and Publisher **[scott.wayne@analog.com].**

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Reducing Ground Bounce in DC-to-DC Converters—Some Grounding Essentials

By Jeff Barrow [jeff.barrow@analog.com]

Electrical ground[1] looks simple on a schematic; unfortunately, the actual performance of a circuit is dictated by its printed-circuit-board (PCB) layout. What's more, ground-node analysis is difficult, especially for dc-to-dc converters, such as *buck* and *boost* circuits, which pound the ground node with large, fast-changing currents. When the ground node moves, system performance suffers and the system radiates EMI. But a well-"grounded" understanding of the physics of ground noise can provide an intuitive sense for reducing the problem.

Ground bounce can produce transients with amplitudes of *volts*; most often changing *magnetic flux* is the cause. A loop of wire carrying current is essentially an electromagnet whose field strength is proportional to the current. Magnetic flux is proportional to the magnetic field passing through the loop area,

$$\text{Magnetic Flux} \propto \text{Magnetic Field} \times \text{Loop Area}$$

or more precisely,

$$\Phi_B = BA\cos\varphi$$

Where the magnetic flux, Φ_B, is the magnetic field, B, passing through a surface loop area, A, at an angle, φ, to the area's unit vector.

A look at Figure 1 gives meaning to the magnetic flux associated with an electric current. A voltage source pushes current through a resistor and around a loop of wire. This current is associated with magnetic flux encircling the wire. To relate the different quantities, think of grabbing the wire with your right hand (applying the *right-hand rule*). If you point your thumb in the direction of current flow, your fingers will wrap around the wire in the direction of the magnetic field lines. As those field lines pass through the loop, their product is *magnetic flux*, directed in this case into the page.

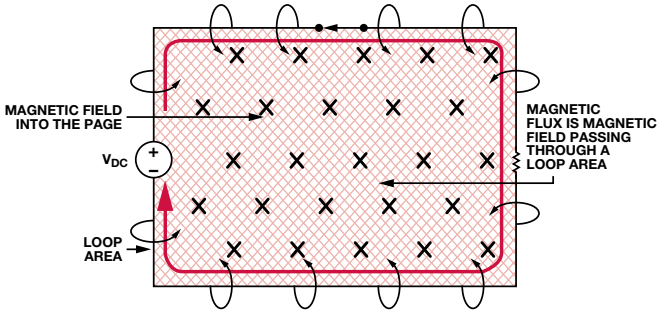


Figure 1. The right-hand rule.

Change either the magnetic field strength or the loop area, and the flux will change. As the flux changes, a voltage is induced in the wire, proportional to the rate of change of the flux, $d\Phi_B/dt$. Notice that either a fixed loop and changing current or a constant current and a changing loop area—or both—will change the flux.

Suppose, for example, that the switch in Figure 2 is suddenly opened. When current stops flowing, the magnetic flux collapses, which induces a momentarily large voltage everywhere along the wire. If part of the wire is a ground return lead, voltage that is supposed to be at ground will spike, thus producing false signals in any circuitry using it as a ground reference.

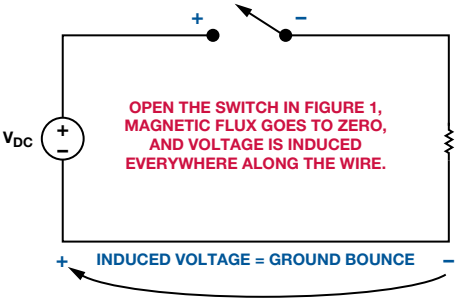


Figure 2. Effect of opening a switch.

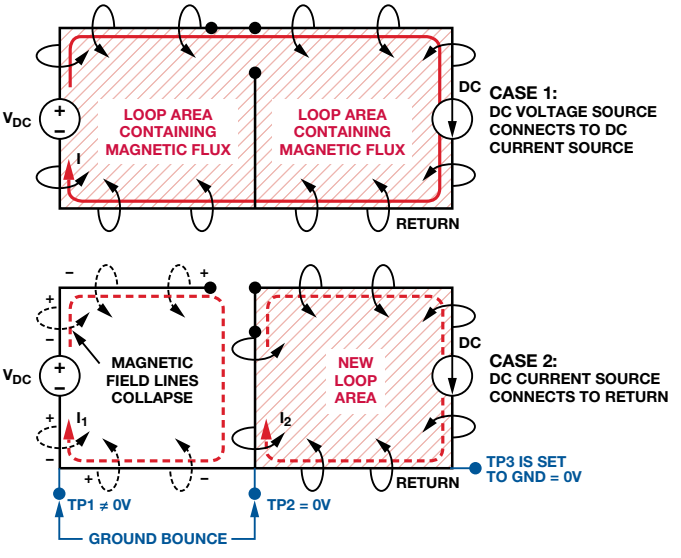
Generally, voltage drops in printed-circuit-board sheet resistance are not a major source of ground bounce. 1-oz copper has a resistivity of about 500 μΩ/square, so a 1-A change in current produces a bounce of 500 μV/square—a problem only for thin, long, or daisy-chained grounds, or precision electronics.

Charging and discharging of parasitic capacitors provides a path for large transient currents to return to ground. The change in magnetic flux from those changing currents induces ground bounce.

The best way to reduce ground bounce in a switching dc-to-dc converter is to control changes in magnetic flux—by minimizing both current loop *areas* and *changes* in loop area.

In some cases, as in Figure 3, the current remains constant, but the switching produces a change of loop *area*, hence a change of flux. In switch Case 1, an ideal voltage source is connected by ideal wires to an ideal current source. Current flows in a loop that includes a ground return.

In Case 2, when the switch changes position, the same current flows in a different path. The current source is dc and does not change, but loop area does change. The change in loop area means a change in magnetic flux, so voltage is induced. Since a ground return is part of that changing loop, its voltage will bounce.



WHEN THE SWITCH CHANGES CASE, THE LOOP AREA CHANGES. EVERYWHERE ALONG THE WIRE IN THE LOWER LEFT, A VOLTAGE IS INDUCED WHERE THE MAGNETIC FIELD COLLAPSES AS I_1 GOES TO 0 AMPS.

Figure 3.

Buck Converter Ground Bounce

For the purpose of discussion, the simple circuit in Figure 3 is similar to—and can be morphed into—the *buck* converter in Figure 4.

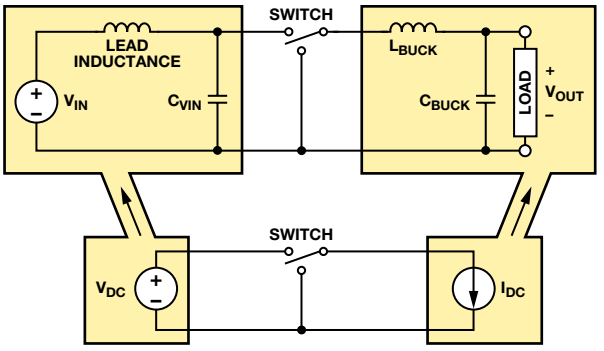


Figure 4. To a high frequency switch, an enormous C_{VIN} and L_{BUCK} look like a voltage and current source.

At high frequencies, a large capacitor—such as the *buck* input capacitor, C_{VIN}—looks like a dc voltage source. Similarly, the large output buck inductor, L_{BUCK}, looks like a dc current source. These approximations are made to help foster intuition.

Figure 5 displays how magnetic flux changes as the switch alternates between the positions.

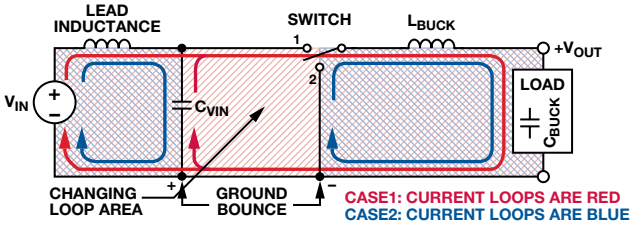


Figure 5. The effect of switching on loop area.

The large L_{BUCK} inductor holds the output current roughly constant. Similarly, C_{VIN} maintains a voltage approximately equal to V_{IN}, so the input current is also more or less constant due to the unchanging voltage across the input lead inductance.

Although the input and output currents are roughly constant, as the switch moves from Position 1 to Position 2, the total loop area rapidly changes in the middle portion of the circuit. That change means a rapid change in magnetic flux, which in turn induces ground bounce along the return wire.

Actual buck converters are made with pairs of semiconductor switches, as shown in Figure 6. Although the complexity has increased with each figure, the analysis of ground bounce induced by changing magnetic flux remains simple and intuitive.

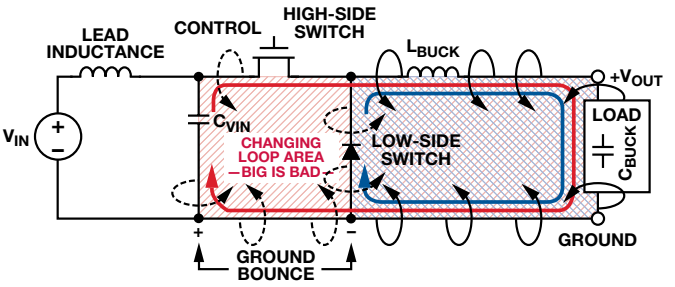


Figure 6. The basic principles are unchanged with semiconductor switching.

The fact that a change in magnetic flux will induce voltage everywhere along a ground return brings up the interesting question: where is true ground? Because ground bounce means a voltage on the ground return trace is bouncing with respect to some ideal point called *ground*, that point needs to be identified.

In the case of power-regulating circuits, true ground needs to be at the low end of the load. After all, a dc-to-dc converter's purpose is to deliver quality voltage and current to the load. All other points along the current return are not ground, just part of the ground return.

Since ground is at the low end of the load, and since changing loop area is the cause for ground bounce, Figure 7 shows how careful placement of C_{VIN} reduces ground bounce by reducing the portion of loop area that changes.

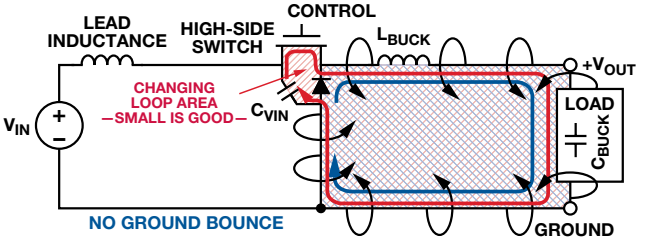


Figure 7. Careful placement of C_{VIN} greatly reduces ground bounce.

Capacitor C_{VIN} bypasses the top of the high-side switch directly to the bottom of the low side switch, thereby shrinking the changing loop area and isolating it from the ground return. From the bottom of V_{IN} to the bottom of the load, no loop-area or switch-current changes occur from one case to the next. Consequently, the ground return does not bounce.

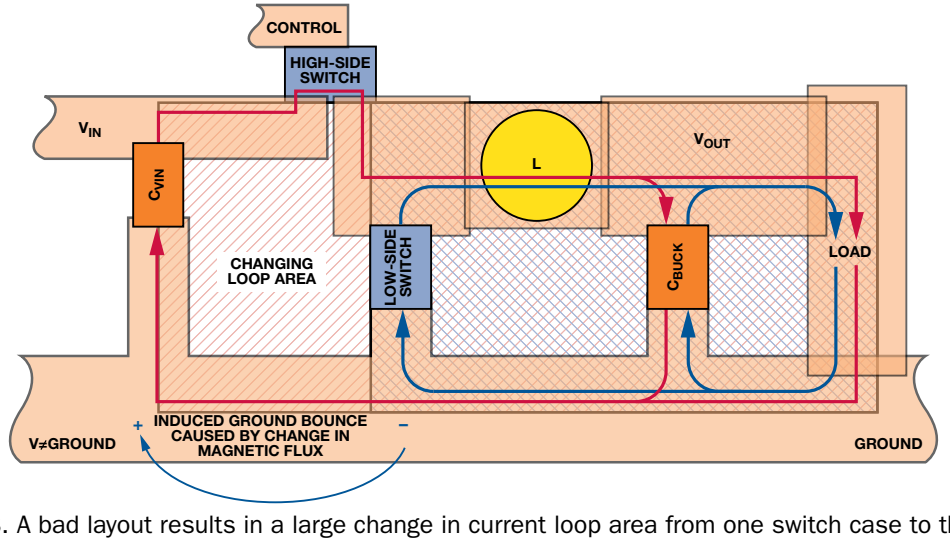


Figure 8. A bad layout results in a large change in current loop area from one switch case to the next.

The PCB layout itself actually determines the performance of the circuit. Figure 8 is a PCB layout of the buck schematic in Figure 6. In the switch position shown in Case 1, with the high-side switch on, dc flow follows the outer red loop. In the switch position shown in Case 2, with the low-side switch on, dc flow now follows the blue loop. Notice the changing loop area, and hence, the changing magnetic flux. So, voltage is induced and the ground bounces.

The layout is realized on a single PCB layer for clarity, but using a second layer of solid ground plane would not fix the bounce. Before showing an improved layout, Figure 9 gives a quick example of where a solid ground plane may not be such a good idea.

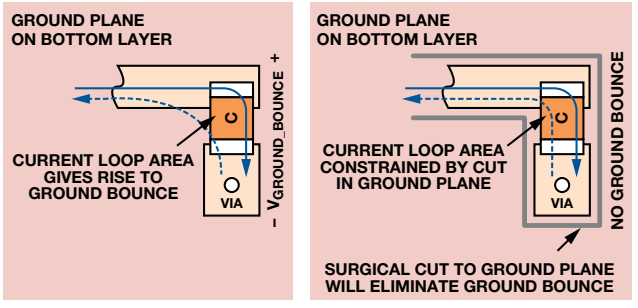


Figure 9. A solid ground plane is not always a good idea.

Here, a 2-layer PCB is constructed so that a bypass capacitor is attached at right angles to a top-layer supply line. In the example on the left, the ground plane is solid and uncut. Top trace current flows through the capacitor, down the via, and out the ground plane.

Because ac always takes the path of least impedance, ground return current rounds the corner on its way back to the source. So the current's magnetic field and the associated loop area change when either magnitude or frequency of the current changes, hence the changing flux. The tendency of current to flow along the easiest path means that even a solid-sheet ground plane can bounce—irrespective of its conductivity.

In the example on the right, a well-planned cut in the ground plane will constrain the return current to a minimum loop area and greatly reduce the bounce. Any residual bounce voltage that is developed in the cut return line is isolated from the general ground plane.

The PCB layout in Figure 10 uses the principle illustrated in Figure 9 to reduce ground bounce. A 2-layer PCB is designed so that the input capacitor and both switches are built over an island in the ground plane.

This layout is not necessarily the best, but it works well and illustrates a key principle. Notice that the loop area enclosed by the red (Case 1) and blue (Case 2) currents is large. However, the difference between the two loops is small. The small change in loop area means a small change in magnetic flux—and so, a small ground bounce. (In general, however, also keep the loop area small—this figure strives to illustrate the importance of matching ac current paths.)

Additionally, in the ground-return island, where magnetic fields and loop area do change, any ground-return bounce is contained by the cut.

Also of interest, the input capacitor, C_{VIN}, may not at first glance appear to be located between the top of the high-side switch and the bottom of the low-side switch, as discussed in Figure 7, but closer perusal will reveal that it is. Although physical proximity can be good, what really matters is the electrical closeness that is achieved by minimizing the area of the loop.

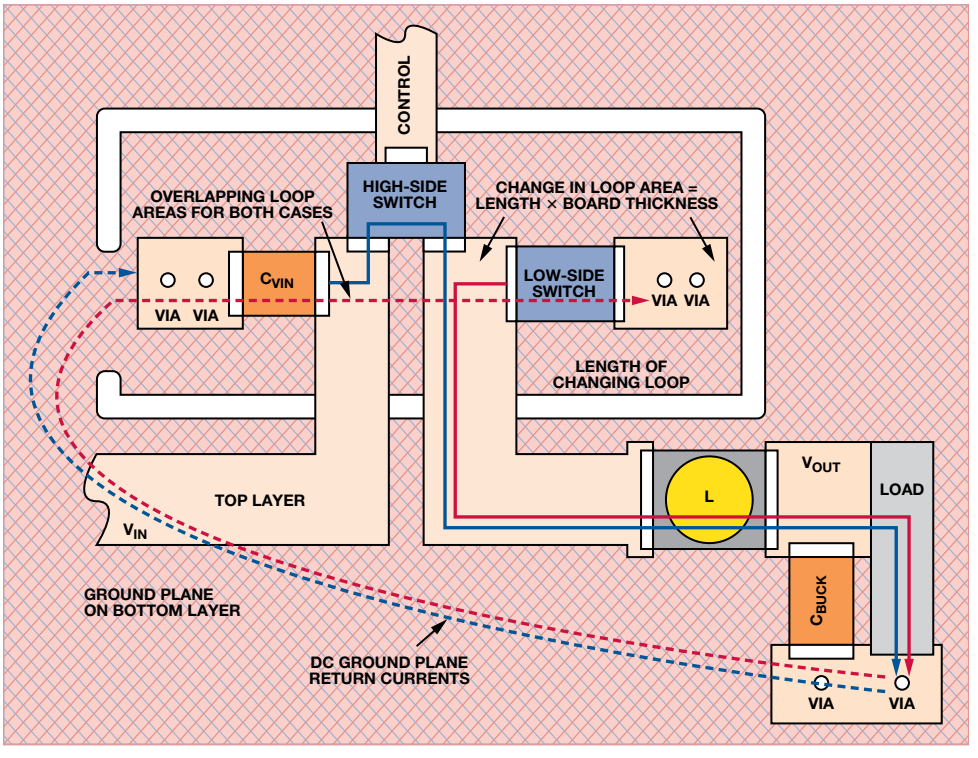


Figure 10. A good buck layout has a small change in loop area as between Case 1 and Case 2.

Boost Converter Ground Bounce

A *boost converter* is essentially a reflection of a buck converter, so—as seen in Figure 11—it is the *output* capacitor that must be placed between the top of the high-side switch and the bottom of the low-side switch to minimize the change in loop area.

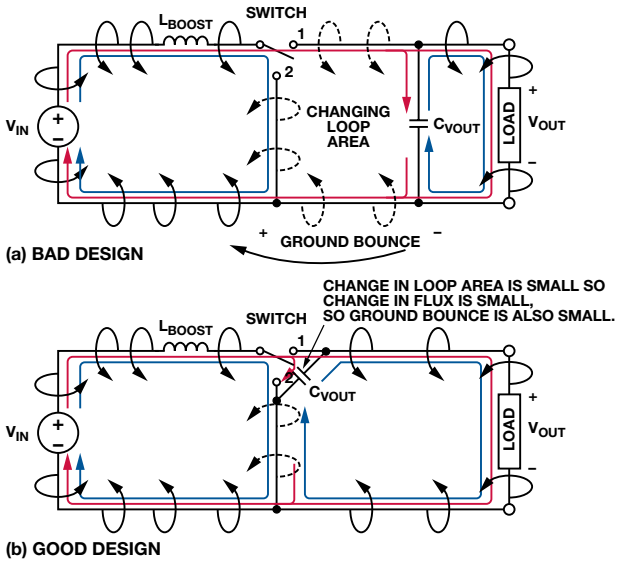


Figure 11. Boost converter means C_{VOUT} placement is critical in the same way that buck converter's C_{VIN} placement is critical. a) Bad design. b) Good design.

Review

Ground-bounce voltage is induced principally by a change in magnetic flux. In a dc-to-dc switching power supply, the flux changes because high-speed switches direct current between different current-loop areas. But careful placement of the buck/boost input/output capacitor and a surgical cut to a ground plane can isolate bounce. However, it is important to be watchful when cutting a ground plane, to avoid possibly increasing the loop area for some other return current in the circuit.

Also, a good layout locates true ground at the bottom of the load, with no changing loop areas or changing currents. Any other conductively associated point may be called "ground," but it is just a point along the return path.

Other Useful Concepts for Ground Analysis

If you keep the following basic ideas in mind, you'll have a good feeling for what will and will not cause ground bounce. Figure 12 shows that conductors that cross at a right angle do not suffer magnetic interaction.

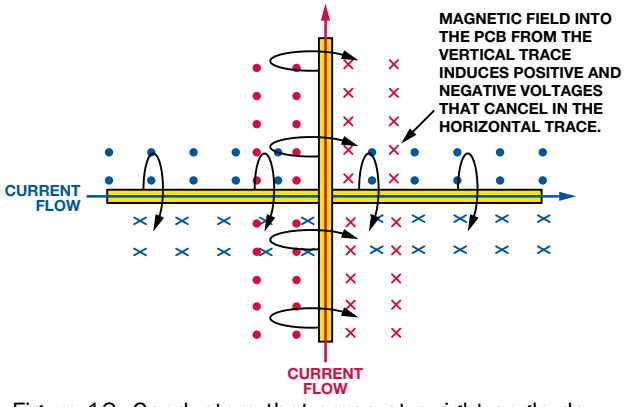


Figure 12. Conductors that cross at a right angle do not interact magnetically.

Magnetic field lines around parallel wires carrying equal currents flowing in the *same* direction cancel everywhere between the wires, so the total stored energy is less than what would be found for the individual wires. For this reason, wide PCB traces have less inductance than narrow traces.

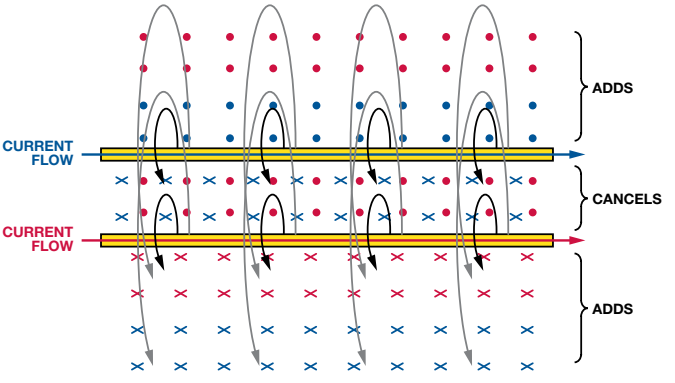


Figure 13. Parallel wires with currents flowing in the same direction.

Magnetic field lines around parallel conductors carrying equal currents flowing in *opposite* directions cancel everywhere outside of the conductors and add everywhere between them. If the inside loop area can be made small, then the total magnetic flux, and therefore the inductance, will also be small. This behavior explains why ac ground plane return current always flows under the top trace conductor.

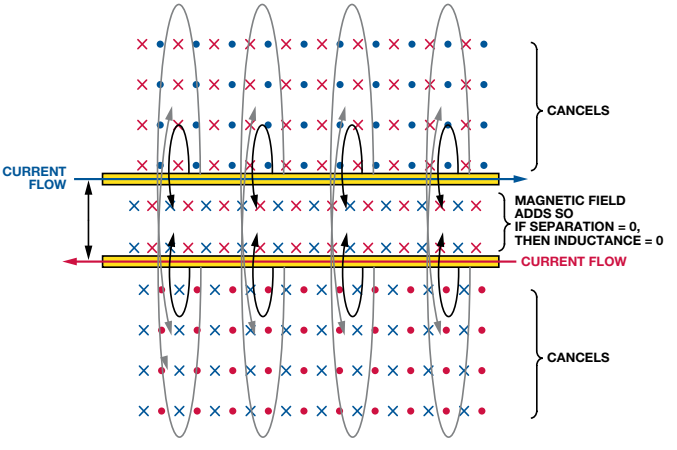


Figure 14. Parallel conductors with currents flowing in opposite directions.

Figure 15 shows why corners increase inductance. A straight conductor sees its own magnetic field, but at a corner, it also sees the magnetic field from the right-angled conductor. As a result, corners store more magnetic energy, and so, have more inductance than straight lines.

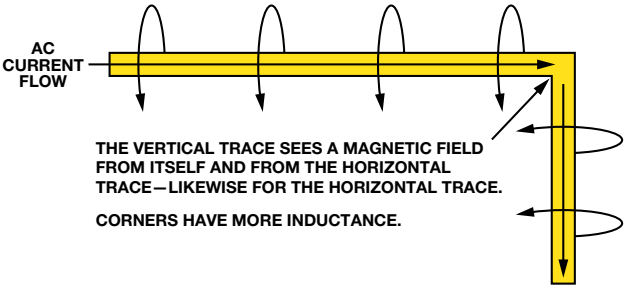


Figure 15. Why corners increase inductance.

Figure 16 shows that interruptions to the ground plane under conductors carrying current can increase loop area by diverting the return current, thus increasing loop size and facilitating ground bounce.

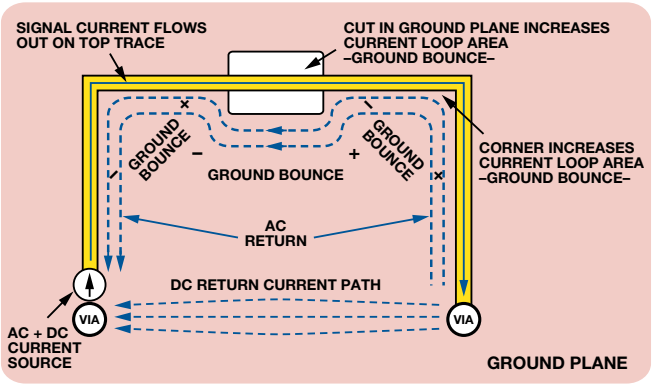


Figure 16. Return current takes the path of least impedance.

Component orientation does matter, as shown in Figure 17.

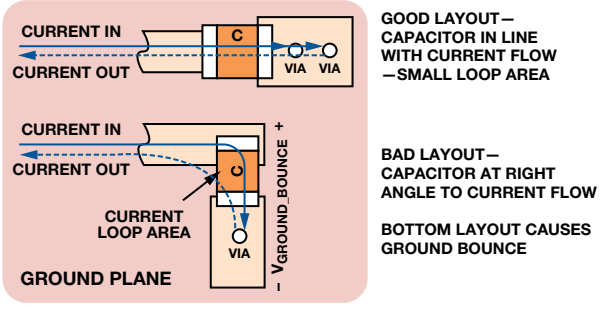


Figure 17. Effects of component orientation.

Summary

Ground bounce is always a potential problem. For a monitor or TV, it can mean a noisy picture—for an audio device, background noise. In a digital system, it can lead to computation errors—even a system crash.

A careful estimation of parasitic elements followed by detailed simulation is a rigorous way to predict the magnitude of ground bounce. But to guide circuit-design intuition, it is necessary to understand the physics underlying its origin.

First, design the PCB so that the low end of the load is the true ground point.

Then, simplify the circuit dynamics by replacing large inductors and capacitors with current- and voltage sources. Look for the current loops in each switching combination. Make the loops overlap; where that is impossible, carefully cut out a small island of ground return such that only dc flows into and out of the opening.

In most cases, these efforts will give acceptable ground performance. If they don't, consider ground-plane resistance, then the displacement currents flowing in parasitic capacitors across all switches and down into the return path.

No matter what the circuit, the basic grounding principles are the same—changing magnetic flux needs to be minimized and/or isolated.

ENDNOTE

[1] Many articles on the problems of "ground" have been published in *Analog Dialogue* and are available in our comprehensive online archive. An article co-authored by Paul Brokaw and the present author in 23-3 (1989) pp. 7-9 appears below in miniature. It includes footnote references to earlier related material on grounding and noise. Related material can be found in 11-2 (1977) pp. 10-15; 25-2 (1991) pp. 24-25; 26-2 (1992) p. 27 (includes a good set of references); 30-2 (1996) p. 11 (a bibliography on EMC/EMI/ESD); 39-3 (2005) pp. 3-8. The book of seminar notes, *High Speed System Applications*, ed. Walt Kester and Hank Zumbahlen, Analog Devices (2006), has an extensive section on PC-board layout and design tools (pp. 4.1-4.90). See also a related earlier article, "Reducing Ground Bounce in DC/DC-Converter Applications," by Jeff Barrow—*EDN*, 7/6/2006.

This article is available in HTML and PDF at *http://www.analog.com/analogdialogue*. Click on *archives*, then select volume, number, and title.

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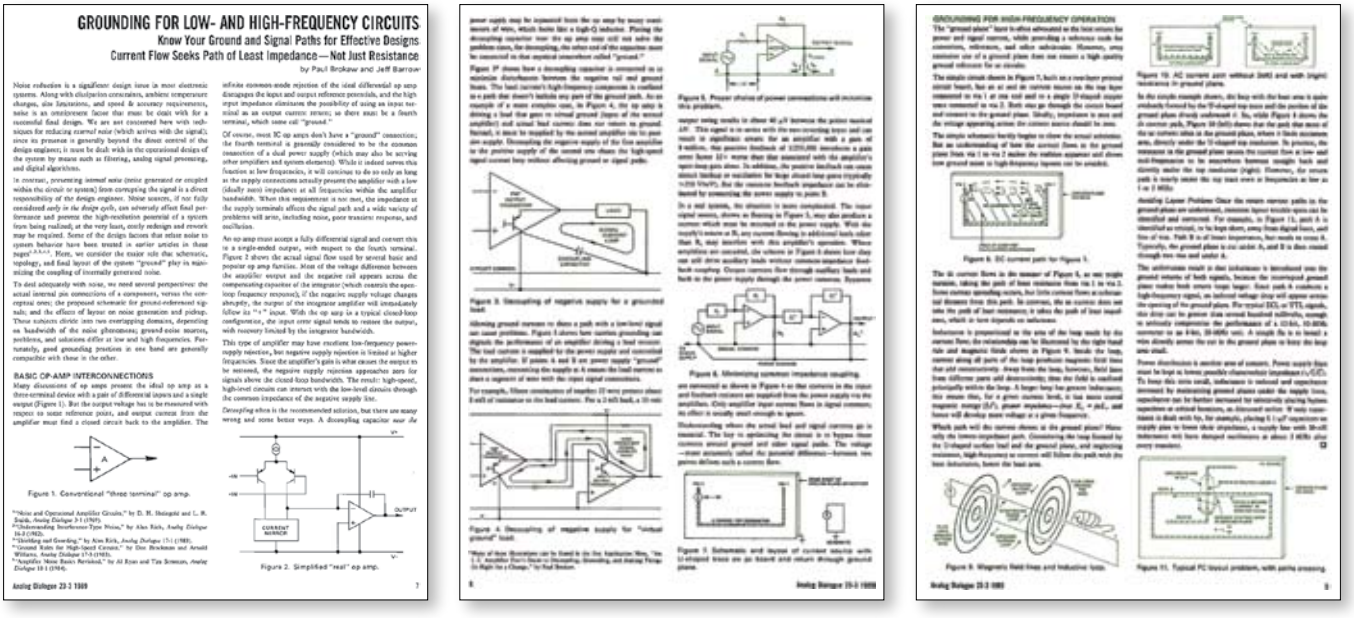

Ask The Applications Engineer—37

Low-Dropout Regulators

By Jerome Patoux [jerome.patoux@analog.com]

This article introduces the basic topologies and suggests good practical usage for ensuring stable operation of *low-dropout voltage regulators* (LDOs). We will also discuss design characteristics of Analog Devices families of LDOs, which offer a flexible approach to maintaining dynamic- and dc stability.

Q: *What are LDOs and how are they used?*

A: Voltage regulators are used to provide a stable power supply voltage independent of load impedance, input-voltage variations, temperature, and time. Low-dropout regulators are distinguished by their ability to maintain regulation with small differences between supply voltage and load voltage. For example, as a lithium-ion battery drops from 4.2 V (fully charged) to 2.7 V (almost discharged), an LDO can maintain a constant 2.5 V at the load.

The increasing number of portable applications has thus led designers to consider LDOs to maintain the required system voltage independently of the state of battery charge. But portable systems are not the only kind of application that might benefit from LDOs. Any equipment that needs constant and stable voltage, while minimizing the upstream supply (or working with wide fluctuations in upstream supply), is a candidate for LDOs. Typical examples include circuitry with digital and RF loads.

A "linear" series voltage regulator (Figure 1) typically consists of a reference voltage, a means of scaling the output voltage and comparing it to the reference, a feedback amplifier, and a series pass transistor (bipolar or FET), whose voltage drop is controlled by the amplifier to maintain the output at the required value. If, for example, the load current decreases, causing the output to rise incrementally, the error voltage will increase, the amplifier output will rise, the voltage across the pass transistor will increase, and the output will return to its original value.

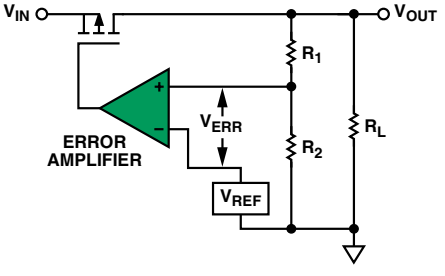

Figure 1. Basic enhancement-mode PMOS LDO.

In Figure 1, the error amplifier and PMOS transistor form a voltage-controlled current source. The output voltage, V_{OUT}, is scaled down by the voltage divider (R_1, R_2) and compared to the reference voltage (V_{REF}). The error amplifier's output controls an enhancement-mode PMOS transistor.

The *dropout voltage* is the difference between the output voltage and the input voltage at which the circuit quits regulation with further reductions in input voltage. It is usually considered to be reached when the output voltage has dropped to 100 mV below the nominal value. This key factor, which characterizes the regulator, depends on load current and junction temperature of the pass transistor.

Q: *How are regulators distinguished by dropout voltage?*

A: We can suggest three classes: standard regulators, quasi-LDOs, and low-dropout regulators (LDOs).

Standard regulators, which typically employ NPN pass transistors, usually drop out at about 2 V.

Quasi-LDO regulators usually use a Darlington structure (Figure 2) to implement a pass device made up of an NPN transistor and a PNP. The dropout voltage, V_{SAT} (PNP) + V_{BE} (NPN), is typically about 1 V—more than an LDO but less than a standard regulator.

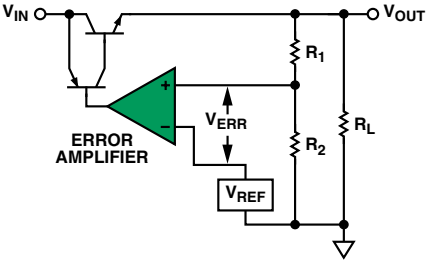

Figure 2. Quasi-LDO circuit.

LDO regulators are usually the optimal choice based on dropout voltage, typically 100 mV to 200 mV. The disadvantage, however, is that the ground-pin current of an LDO is usually higher than that of a quasi-LDO or a standard regulator.

Standard regulators have a higher dropout voltage and dissipation, and lower efficiency, than the other types. They can be replaced by LDO regulators much of the time, but the maximum input voltage specification—which can be lower than that for standard regulators—should be considered. In addition, some LDOs will need specially chosen external capacitors to maintain stability. The three types differ somewhat in both bandwidth and dynamic stability considerations.

Q: *How can I select the best regulator for my application?*

A: To choose the right regulator for a specific application, the type and range of input voltage (e.g., the output voltage of the dc-to-dc converter or switching power supply ahead of the regulator), needs to be considered. Also important are: the required output voltage, maximum load current, minimum dropout voltage, quiescent current, and power dissipation. Often, additional features may be useful, such as a shutdown pin or an error flag to indicate loss of regulation.

The source of the input voltage needs to be considered in order to choose a suitable category of LDO. In battery-powered applications, LDOs must maintain the required system voltage as the battery discharges. If the dc input voltage is provided from a rectified ac source, the dropout voltage may not be critical, so a standard regulator—which may be cheaper and can provide more load current—could be a better choice. But an LDO could be the right choice if lower power dissipation or a more precise output voltage is necessary.

The regulator should, of course, be able to provide enough current to the load with specified accuracy under worst-case conditions.

LDO Topologies

In Figure 1, the pass device is a PMOS transistor. However, a variety of pass devices are available, and LDOs can be classified depending on which type of pass device is used. Their differing structures and characteristics offer various advantages and drawbacks.

Examples of four types of pass devices are shown in Figure 3, including NPN and PNP bipolar transistors, Darlington circuits, and PMOS transistors.

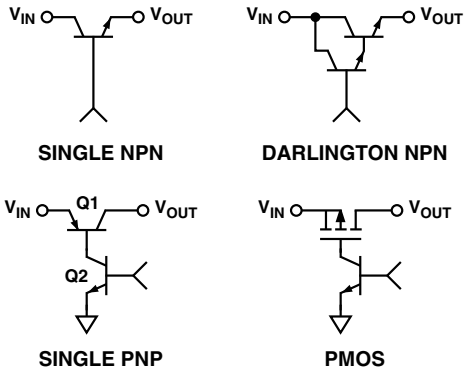

Figure 3. Examples of pass devices.

For a given supply voltage, the bipolar pass devices can deliver the highest output current. A PNP is preferred to an NPN, because the base of the PNP can be pulled to ground, fully saturating the transistor if necessary. The base of the NPN can only be pulled as high as the supply voltage, limiting the minimum voltage drop to one V_{BE}. Therefore, NPN and Darlington pass devices can't provide dropout voltages below 1 V. They can be valuable, however, where wide bandwidth and immunity to capacitive loading are necessary (thanks to their characteristically low Z_{OUT}).

PMOS and PNP transistors can be effectively saturated, minimizing the voltage loss and the power dissipated by the pass device, thus allowing low dropout, high-efficiency voltage regulators. PMOS pass devices can provide the lowest possible dropout voltage drop, approximately $R_{DS(ON)} \times I_L$. They also allow the quiescent current flow to be minimized. The main drawback is that the MOS transistor is often an external component—especially for controlling high currents—thus making the IC a *controller*, rather than a complete self-contained regulator.

The power loss in a complete regulator is

$$P_D = (V_{IN} - V_{OUT})\, I_L + V_{IN} I_{GND}$$

The first part of this relationship is the dissipation of the pass device; the second part is the power consumption of the controller portion of the circuit. The ground current in some regulators, especially those using saturable bipolar transistors as pass devices, can peak during power-up.

Q: *How can LDO dynamic stability be ensured?*

A: Classical LDO circuit designs for general-purpose applications have problems with stability. The difficulties stem from the nature of their feedback circuits, the wide range of possible loads, the variability of elements within the loop, and the difficulty of obtaining precision compensation devices with consistent parameters. These considerations will be discussed below, followed by a description of the anyCAP® circuit topology, which has improved stability.

LDOs generally use a feedback loop to provide a constant voltage, independent of load, at the output. As is true for any high-gain feedback loop, the location of the poles and zeros in the loop-gain transfer function will determine the stability.

NPN-based regulators, with their low-impedance emitter-loaded output, tend to be relatively insensitive to output capacitive loading. PNP and PMOS regulators, however, have higher output impedance (collector loaded in the case of the PNP). In addition, the loop's gain and phase characteristics strongly depend on the load impedance, thus requiring special consideration for stability.

The transfer function of PNP- and PMOS-based LDOs has several poles that impact stability:

- The dominant pole (*P0* in Figure 4) is set by the error amplifier; it is controlled and fixed, in conjunction with the g_m of the amplifier, through an internal compensation capacitance C_{COMP}. This pole is common to all of the LDO topologies described above.
- The second pole (*P1*) is set by the output elements (the combination of the output capacitance and the load capacitance and resistance). This makes the application problem more difficult to handle, as these elements affect both the loop gain and bandwidth.
- A third pole (*P2*) is due to parasitic capacitance around the pass elements. PNP power transistors have a unity-gain frequency (f_T) much lower than that of comparable NPN transistors, under the same conditions.

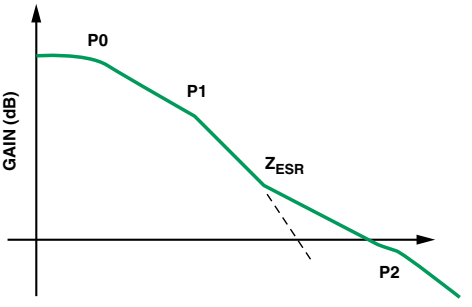

Figure 4. LDO frequency amplitude response.

As Figure 4 shows, each pole contributes 20 dB/decade of roll-off in gain, with up to 90° of phase shift. As the LDOs discussed here have multiple poles, the linear regulator will be unstable if the phase shift at the unity-gain frequency approaches –180°. Figure 4 also shows the effect of loading the regulator with a capacitor, whose *effective series resistance* (ESR) will add a zero (Z_{ESR}) into the transfer function. This zero will help to compensate for one of the poles and can help to stabilize the loop if it occurs below the unity-gain frequency and keeps the phase shift well below –180° at that frequency.

ESR can be critical for stability, especially for LDOs with vertical-PNP pass devices. As a parasitic property of a capacitor, however, the ESR is not always well-controlled. A circuit may require the ESR to fall within a certain window to ensure that the LDO operates in the stable region for all output currents (Figure 5).

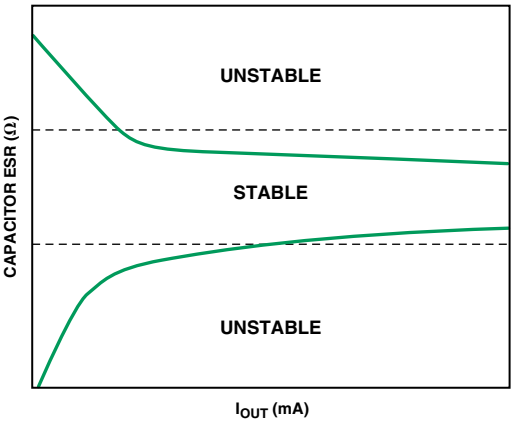

Figure 5. Stability as a function of output current and load-capacitor ESR.

Even in principle, choosing the right capacitor with the right ESR (high enough to reduce the slope before the frequency response crosses through 0 dB, yet low enough to bring the gain below 0 dB before the associated pole, *P2*) can be challenging. Yet the practical considerations add further challenges: ESR varies, depending on the brand; and the minimum capacitance value to use in production will require bench tests, including extreme cases with minimum ambient temperature and maximum load. The choice of the type of capacitor is also important. Perhaps the most suitable are tantalum capacitors, despite their large size in the higher-capacitance ranges. Aluminum electrolytics are compact, but their ESR tends to deteriorate at low temperatures, and they don't work well below –30°C. Multilayer ceramic types do not have sufficient capacitance for conventional LDOs (but they are suitable for anyCAP designs, read on).

Analog Devices anyCAP family of LDOs

LDO implementation is considerably easier now, thanks to improvements in both dc and ac performance associated with regulators employing the Analog Devices anyCAP LDO architecture. As the term implies, regulators embodying it are relatively insensitive to both the size of the capacitor and its ESR, thus allowing for a wider possible range of output capacitance. The approach has spread and is now more widely available in the marketplace, but it may be helpful to understand how this architecture (Figure 6) simplifies the stability issue.

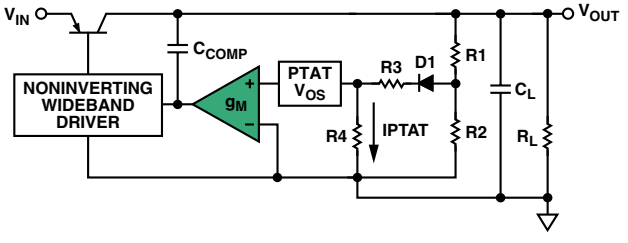

Figure 6. Simplified schematic of anyCAP LDO.

The anyCAP family of LDOs, including the 100-mA ADP3307[1] and the 200-mA low-quiescent-current ADP3331,[2] can remain stable with output capacitance as low as 0.47 µF, using good-quality capacitors of any type, including compact multilayer ceramic. ESR is essentially a nonissue.

The simplified schematic of Figure 6 shows how a single loop provides both regulation and reference functions. The output is sensed by the external R1-R2 voltage divider, and fed back to the input of a high-gain amplifier through diode D1 and the R3-R4 divider. At equilibrium, the amplifier produces a large, repeatable, well-controlled offset voltage that is *proportional to absolute temperature* (PTAT). This voltage combines with the complementary temperature-sensitive diode voltage drop to form the implicit reference, a temperature-independent virtual band-gap voltage.

The amplifier output connects to an unusual noninverting driver that controls the pass transistor, allowing the frequency compensation to include the load capacitor in a pole-splitting arrangement based on Miller compensation. This provides reduced sensitivity to value, type, and ESR of the load capacitor. Additional advantages of the pole-splitting scheme include superior line-noise rejection and very high regulator gain, thereby providing exceptional accuracy and excellent line and load regulation.

Q: *Would you discuss the Analog Devices families of LDOs?*

A: The choice of LDO depends, of course, on the supply voltage range, load voltage, and required maximum dropout voltage. The main differences between devices focus on power consumption, efficiency, price, ease of use, and the various specifications and packages available.

The popular ADP33xx anyCAP family of ADI LDOs has been on the market for several years. Based on a BiCMOS process and a PNP pass transistor, it allows good regulation and many of the advantages mentioned above, but tends to be somewhat more expensive than CMOS parts.

Some recent designs, such as the ADP17xx family, are entirely CMOS-based, with a PMOS pass transistor, which allows the fabrication of LDOs at lower cost, but with a trade-off on line-regulation performance. Devices in this family can handle a large range of output capacitance, but they still require at least 1 µF and ≤500-mΩ ESR. For example, the 150-mA ADP1710[3] and ADP1711[4] are optimized for stable operation with small 1-µF ceramic output capacitors, allowing for good transient performance while occupying minimal board space, and the 300-mA ADP1712,[5] ADP1713,[6] and ADP1714[7] can use ≥2.2-µF capacitors.

Both of these families have 16 fixed-output-voltage options, from 0.75 V to 3.3 V, as well as an adjustable-output option in the 0.8-V to 5-V range. Accuracy is to within ±2% over line, load, and temperature. The ADP1711 and ADP1713 fixed-voltage versions allow for a reference-bypass capacitor to be connected; this reduces output voltage noise and improves power-supply rejection. The ADP1714 includes a tracking feature, which allows the output to follow an external voltage rail or reference. Dropout voltages at rated load are 150 mV for the ADP1710 and ADP1711; and 170 mV for the ADP1712, ADP1713, and ADP1714. Power-supply rejection (PSR) is high (69 dB and 72 dB at 1 kHz), and power consumption is low, with ground current of 40 µA and 75 µA with 100-µA load.

Typical transient responses of the ADP1710 and ADP1711 are compared in Figure 7 for a nearly full-load step, with 1-µF and 22-µF input- and output capacitors.

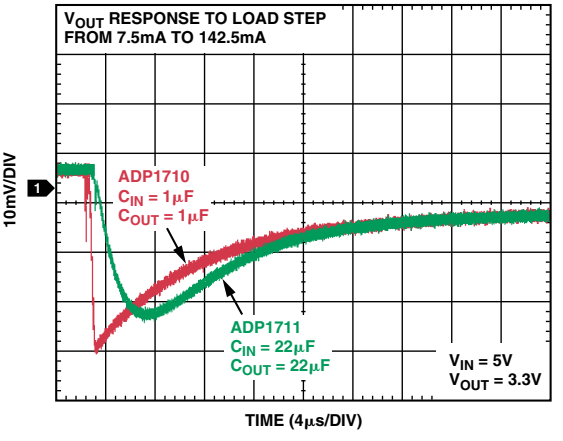

Figure 7. Transient response of ADP1710/ADP1711.

The operating junction temperature range is –40°C to +125°C. Both families are available in tiny 5-lead TSOT packages, a small-footprint solution to the variety of power needs.

REFERENCES—VALID AS OF JULY 2007

[1]ADI website: www.analog.com (Search) ADP3307 (Go)
[2]ADI website: www.analog.com (Search) ADP3331 (Go)
[3]ADI website: www.analog.com (Search) ADP1710 (Go)
[4]ADI website: www.analog.com (Search) ADP1711 (Go)
[5]ADI website: www.analog.com (Search) ADP1712 (Go)
[6]ADI website: www.analog.com (Search) ADP1713 (Go)
[7]ADI website: www.analog.com (Search) ADP1714 (Go)

PRODUCT INTRODUCTIONS: VOLUME 41, NUMBER 2

Data sheets for all ADI products can be found by entering the model number in the Search box at www.analog.com

April

ADC, Successive-Approximation, 18-bit, 1-MSPS, 7-mW power consumption **AD7982**
Comparator, Voltage, dual-polarity outputs, reference **ADCMP361**
Comparator, Voltage, dual, reference **ADCMP670**
Comparators, Voltage, dual, programmable-hysteresis, reference **ADCMP34x**
DAC, Current Output, 10-bit, 120-mA output current **AD5821**
DACs, Voltage Output, quad, 12-/14-/16-bit, 5-ppm/°C reference **AD56x5R**
DACs, Voltage Output, quad, 12-/16-bit, $I^2C^®$ interface **AD5625/AD5665**
Isolators, Digital, 2-channel, 50-mW dc-to-dc converter **ADuM524x**
Processors, Audio, for advanced TV **ADAV4101/ADAV4201**
Processors, Audio, for advanced TV **ADAV43x2/ADAV44x2**
Switch, CMOS, multimedia **ADG790**
Synthesizer, Frequency, integer-N PLL, high-voltage charge pump **ADF4113HV**

May

Driver, Half-Bridge, isolated, 100-mA output current **ADuM1233**
Gyroscope, low-power, programmable **ADIS16255**
Gyroscope, yaw-rate **ADXRS612**
Regulator, Linear, micropower, 50-mA output **ADP1720**
Transceiver, high-performance, narrow-band, ISM band **ADF7021**
Transmitter, HDMI/DVI, high-performance **AD9889B**
Voltage Monitor/Sequencer, quad **ADM1185**

June

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ADC, Sigma-Delta, 20-bit, 3-channel, in-amp, reference **AD7785**
Amplifier, Audio, Class-D, 2-W, filterless, stereo **SSM2306**
Amplifier, Instrumentation, programmable-gain, high-precision **AD8231**
Amplifier, Instrumentation, programmable-gain, 10-MHz bandwidth **AD8251**
Amplifier, Operational, dual, low-noise, low-power, precision **AD8667**
Amplifier, Operational, dual, low-power, high-precision, auto-zero **AD8539**
Amplifiers, Operational, low-cost, JFET-input, precision **ADA4000-x**
Codec, Audio, 24-bit, 192-kHz, PLL, four ADCs, digital audio output **AD1974**
Codec, Audio, 24-bit, 192-kHz, PLL, two ADCs, eight DACs **AD1928**
Codec, Audio, high-definition audio **AD1987**
Comparator, Voltage, fast, low-power, single-supply, rail-to-rail **ADCMP608**
Converter, Synchronous Buck, 2-/3-phase, 8-bit VID code, Intel **ADP3193A**
DAC, Voltage-Output, quad, 12-bit, unipolar or bipolar outputs **AD5726**
Driver, ADC, differential, extremely low harmonic distortion **ADA4937-1**
Drivers, Differential, triple, high-resolution component video **AD814x**
Front-End, mixed-signal, broadband modem **AD9868**
Generator, Clock, 14-output, on-chip VCO **AD9516-x**
Gyroscope, low-power, programmable **ADIS16251**
Gyroscopes, yaw-rate **ADXRS61x**
Isolators, Digital, 2-channel, hot-swappable, I^2C, 5-kV **ADuM2250/ADuM2251**
Microcontrollers, Analog, PWM generator, H-bridge motor control **ADuC7128/ADuC7129**
Modulators, Quadrature, 869-MHz to 960-MHz/ 1805-MHz to 1990-MHz **ADL5590/ADL5591**
Monitor, Current-Shunt, high-voltage **AD8212**
Monitor, Current-Shunt, high-voltage, dual **AD8213**
Multiplexer/Demultiplexer, 1:2/2:1, 3.2-Gbps **AD8153**
Output Stage, Power, 2-channel, Class-D audio-amplifier **ADAU1513**
Reference, Voltage, 1.25-V, precision, micropower, shunt-mode **ADR1581**
Signal Splitter, Active, RF, 1:2, single-ended **ADA4304-2**
Switch, Crosspoint, 4 × 4, 6.25-Gbps, input equalization **AD8156**
Switch, Crosspoint, 32 × 32, buffered, video, 600 MHz **AD8118**
Switch, Crosspoint, triple 16 × 9, buffered, video, 500 MHz **AD8175**

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Adam Champy joined Analog Devices in 2005 as an applications engineer in the Micromachined Products Division, where he supports accelerometer applications in automotive safety systems, video games, and portable handsets. Prior to joining ADI, Adam attended MIT, earning master's and bachelor's degrees in electrical engineering and computer science. For his thesis, he designed an embedded control system for a mass-spectrometer sensor employed in submarine-based environmental research.

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